A Single DC Source Cascaded Seven-Level Inverter Integrating Switched-Capacitor Techniques

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***Abstract*—In this paper, a novel cascaded seven-level inverter topology with a single input source integrating switched-capacitor techniques is presented. Compared with the traditional cascade multilevel inverter, the proposed topology replaces all the separate dc sources with capacitors, leaving only one H-bridge cell with a real dc voltage source and only adds two charging switches. The capacitor charging circuit contains only power switches, so that the capacitor charging time is independent of the load. The capacitor voltage can be controlled at a desired level without complex voltage control algorithm and only use the most common carrier phase-shifted sinusoidal pulse width modulation strategy. The operation principle and the charging–discharging characteristic analysis are discussed in detail. A 1-kW experimental prototype is built and tested to verify the feasibility and effectiveness of the proposed topology.**

***Index Terms*—Carrier phase-shifted sinusoidal pulse width modulation (CPS-SPWM), cascaded seven-level inverter, charging and discharging characteristic, switched-capacitor techniques.**

I. Introduction

MULTILEVEL converters are finding considerable attention in academia and industry as one of the preferred choices for high-power conversion applications, such as traction drives, active filters, reactive power compensators, photovoltaic power conversion, uninterruptible power supplies, static compensators, and flexible ac transmission systems [1]–[4]. In general, multilevel converters are classified into diode-clamped [5], flying capacitor [6], and cascaded multilevel inverter topologies [7]. A particular attention has been given to cascaded multilevel topology because of its modularity, symmetrical structure, and simplicity of control.

However, the main drawback with the cascade multilevel inverter (CMI) is the large amount of separate isolated sources required to feed each of the H-bridges. It will need n isolated sources for $2n + 1$ levels of output. Photovoltaic panel, fuel cells, batteries, and ultracapacitors are the most common independent sources. A five-level CMI for distributed energy applications is presented in [8]. The input ports of the CMI are connected to photovoltaic (PV) modules. However, PV output power depends on weather conditions, such as irradiation and temperature, and it is unavailable at night, which implies that the system cannot work at night. A galvanic isolated charger for the PV port should be installed in the CMI system by connecting to an existing storage unit port. However, this consequently increases the complexity and cost of the system. In [9], the CMI input ports are connected to a group of batteries, whose characteristics are large size, high cost, and the battery discharging speed limits the continuity of the system.

Some solutions to reduce the number of isolated source in the CMI are proposed. An important improvement is the "asymmetrical CMI" (ACMI), which can generate the same number of levels with fewer power supplies [10]. ACMI increases the power quality, but they lose modularity and still need more than one isolated sources. Control and hardware strategies for a 27-level ACMI are proposed to reduce the nine power supplies to only four, all of them unidirectional [11]. An ACMI with a single dc voltage source employing a cascaded transformer is introduced in [12]. However, the transformer makes the system bulky because it operates in a low frequency. A different approach using only one power source has been implemented in [13]. To eliminate the dc sources of the auxiliary converters, the system uses a high-frequency link (HFL), based on a square-wave generator and a multiwinding toroidal transformer. However, the size of the HFL must be big enough to supply the 20% of the power required by the machine. With an appropriate modulation adjustment in [14], the size of the HFL can be minimized to less than 2%.

However, the isolated dc sources in these solutions have to be fed from isolation transformers, which are more expensive and bulky. An alternative option without transformers is to replace all the separate dc sources feeding the H-bridge cells with capacitors, leaving only one H-bridge cell with a real dc voltage source. However, a complex voltage control algorithm is required to keep the capacitor voltage controlled at the desired level. The researchers have proposed various efficient control algorithms. The proposed method in [15] and [16] uses the switching state redundancy for capacitor voltage regulation in inductive load. However, the output current of the converter as well as the time duration of the redundant switching states greatly impact the charging and discharging patterns of the replacing capacitors. A simple capacitor voltage regulation

Manuscript received August 31, 2015; revised November 29, 2015 and January 21, 2016; accepted February 19, 2016. Date of publication April 21, 2016; date of current version October 7, 2016.

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Digital Object Identifier 10.1109/TIE.2016.2557317

constraint is derived which can be used in optimization problems for harmonic minimization or harmonic mitigation to guarantee capacitor voltage regulation in all load condition [17]. A new control method, phase-shift modulation, is used to regulate the voltage of the capacitors replacing the independent dc source. The method is robust and does not incur much computational burden [18]. The proposed dc-voltage-ratio control in [19] is based on a time-domain modulation strategy that avoids the use of inappropriate states to achieve any dc voltage ratio. The following are the three associated problems of this topology: 1) regulating the voltage across the capacitors makes the controller design complex, 2) the charging circuit contains the load. Thus, the charging time and the capacitor voltage are affected by the load variation, and 3) the charging–discharging characteristics and efficiency issues of the capacitor are not fully discussed in the literature.

The efficiency of switched-capacitor in dc–dc converters has been a widely debated issue among researchers [20]–[22]. The equations for the relationship between peak current and circuit's parameters are presented in [23]. With the method, the high pulse current at charging transient can be limited to obtain a higher efficiency. In [24], the efficiency of a *RC* circuit under different conditions in the charging and discharging operation is analyzed systematically. Based on the analysis, some design rules useful for developing high-efficiency switched-capacitor converters are suggested. Resonant switched-capacitor converter using small inductors is also considered as a promising approach to avoid the drawback of the spike current [25].

In this paper, a novel cascaded seven-level inverter topology with a single input source integrating switched-capacitor techniques is proposed. The proposed topology consists of a charging circuit and three H-bridge inverter units, as shown in Fig. 1(a). The reliable source port U_{in2} can charge capacitor C_1 or C_3 through the charging switch and H-bridge switches simultaneously and individually. The charging circuit contains only power switches and capacitors, so that the charging time is independent of the load. The capacitor voltage can be controlled at a desired level with transformerless charging technique and without complex voltage control algorithm.

The proposed structure can be used for a photovoltaic-battery three-input inverter application, as shown in Fig. 1(b). When the photovoltaic ports are available, the converter is used as a traditional cascaded seven-level inverter with three independent isolated sources [7]. However, in the case PV ports powering OFF in the night, all the separate PV sources are separated from the converter and are replaced by capacitors, so that the operation principle is the same as the converter in Fig. 1(a). With the switched-capacitor techniques, the different H-bridges can share the input source; thus, the redundancy of the topology is enhanced.

This paper is organized as follows. After the Introduction, the carrier phase-shifted sinusoidal pulse width modulation (CPS-SPWM) strategy in the proposed single-supply cascaded seven-level inverter is explained in Section II. The capacitor charging and discharging characteristic are presented in Section III. Section IV analyzes the charging current and loss and the charging-switch pair voltage. Section V presents the simulation and experimental results. Section VI provides the conclusions.

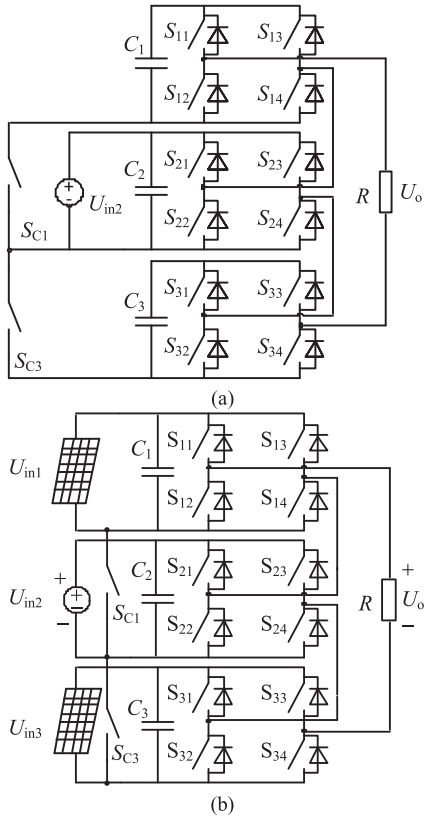

Fig. 1. Topologies of the proposed inverter. (a) The novel single dc source cascaded seven-level inverter. (b) Three-input cascaded seven-level inverter for PV systems.

II. Modulation Strategy

Different multilevel modulation techniques have been presented in the literature. For the CMI, CPS-SPWM is the most common strategy [1], with an improved harmonic performance. The CPS-SPWM associates a pair of carriers to each cell of the CMI, and a phase shift among the carriers of the different cells is introduced. In this way, a stepped multilevel waveform is originated. There are some interesting features and advantages: 1) The output voltage has a switching pattern with $2N$ times the switching frequency (where N is the number of cells). Hence, better total harmonic distortion (THD) is obtained at the output, using $2N$ times lower frequency carriers. 2) Since all the cells are controlled with the same reference and same carrier frequency, the power is evenly distributed among the cells across the entire modulation index [26]. 3) For the single-supply CMI using capacitors, the advantage is that the capacitors are properly charged without complex voltage balancing control algorithm.

The level-shifted SPWM has better output voltage harmonic profile since all the carriers are in phase compared to CPS-PWM. However, this method is not preferred for CMI, since it causes an uneven power distribution among the different cells.

Selective harmonic elimination is a low switching frequency (below 1 kHz) PWM method developed to ensure the elimination of undesired low-order harmonics [26]. Space vector modulation (SVM) exhibits features of good dc-link voltage utilization, better fundamental output voltage, better harmonic performance, and easier implementation in digital signal processor. However, SVM-based algorithms are not the dominant modulation scheme for n-level (n>5) inverter. The number of the voltage vector is increased to 7^3 in seven-level inverter and the calculation of the duration of the voltage vectors is so complicated.

In this paper, CPS-SPWM is performed to obtain the sinusoidal output voltage in the single-supply cascaded seven-level inverter, and the capacitors are charged by introducing charging-switch pairs every cycle. To some extent, capacitor voltage U_{C1} and U_{C3} are regarded as constants, and the three H-bridge inverter cells share balanced power.

The waveforms of the driving signal are given in Fig. 2. Six-way phase-shifted triangular carrier voltages and one-way sinusoidal modulation wave are required for the CPS-SPWM scheme. $Z_1, -Z_1, Z_2, -Z_2, Z_3$, and $-Z_3$ are the carrier signals for $S_{11}, S_{13}, S_{21}, S_{23}, S_{31}$, and S_{33}, respectively, and T_S is the carrier period. A straight line with value $m(0 < m < 1)$ can be substituted for the modulation wave in a carrier cycle, where the carrier frequency is significantly greater than the modulation frequency. The power switches are turned ON when the corresponding carrier wave signal is less than the modulation sine wave m. On the contrary, the switches are OFF when the carrier wave is greater than m. The switches $S_{11}/S_{12}, S_{13}/S_{14}, S_{21}/S_{22}, S_{23}/S_{24}, S_{31}/S_{32}$, and S_{33}/S_{34} are operated in a complementary manner. S_{C1} and S_{C3} are the charging switches. The gate signal of S_{C1} can be obtained with S_{13} and S_{21} by the AND circuit and that of S_{C3} can be obtained with S_{23} and S_{31} by the same circuit. There are 20 kinds of operating status of each switch, as illustrated in Table I and 6 of them are for the charging process and 9 switching status are for the discharging process.

III. Capacitor Charging and Discharging Characteristic Analysis

A. Capacitor Charging State Analysis

Through the charging switch and H-bridge switches, C_1 and C_3 can be charged by the reliable source U_{in2}. From Status 1, Status 2, and Status 3 in Table I, we can see that there is only one charging path for C_1. In other words, the capacitor charging current i_{C1} only goes through S_{21} and S_{13}, as drawn in red color in Fig. 3. According to Status 4–Status 6, we can see that charging current i_{C3} flows through S_{23} and S_{31}. The equivalent charging circuit for C_3 is shown in blue color in Fig. 3.

B. Capacitor Charging Time Analysis

The capacitor charging time is related to the modulation sine wave value m. For simplicity, the charging time for C_1 is taken as an example to have a detailed analysis. When $m \in (0, 2/3)$, the modulation wave $-Z_1$ lags behind Z_2 by $T_S/6$, as shown in

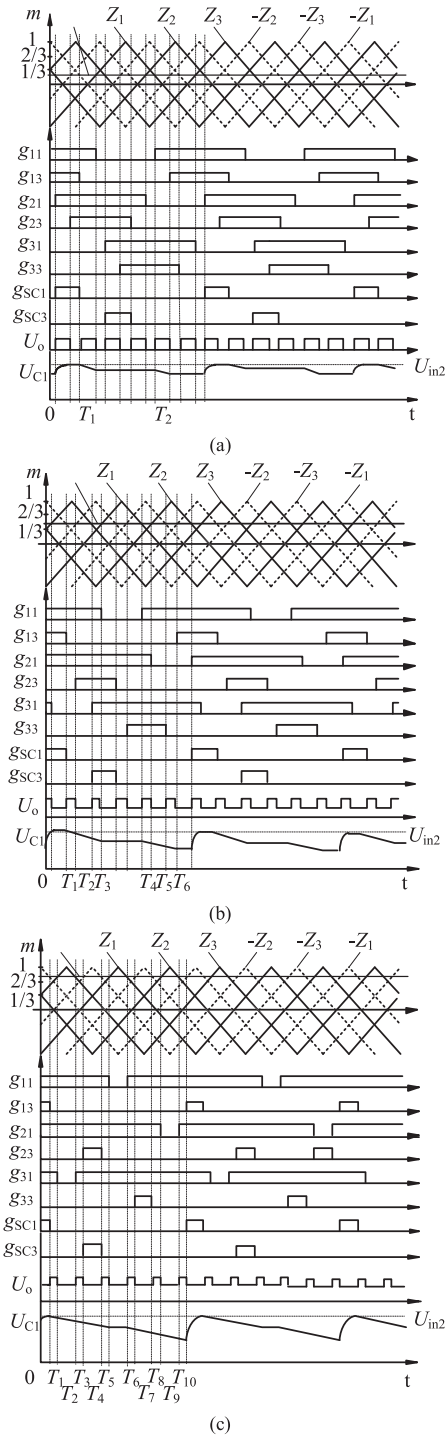

Fig. 2. Waveforms of the driving signal when CPS-SPWM is employed. (a) $m \in (0, 1/3)$ (b) $m \in (1/3, 2/3)$. (c) $m \in (2/3, 1)$.

Fig. 2(a) and (b). At this stage, the falling edge of g_{13} and the rising edge of g_{21} move forward or backward with the variation in m. However, the overlapping portions of g_{13} and g_{21} remain unchanged; thus, the charging time remains $T_S/6$. The output voltage of the inverter is 0 or U_{in2} when $m \in (0, 1/3)$, as illustrated in Fig. 2(a), and U_{in2} or $2\,U_{in2}$ when $m \in (1/3, 2/3)$, as illustrated in Fig. 2(b). When $m \in (2/3, 1)$, S_{21}

TABLE I
OPERATING STATUS OF EACH SWITCH

		S_{11}	S_{13}	S_{21}	S_{23}	S_{31}	S_{33}	S_{C1}	S_{C3}
Charging status	Status 1	1	1	1	0	0	0	1	0
	Status 2	1	1	1	1	0	0	1	0
	Status 3	1	1	1	0	1	0	1	0
	Status 4	0	0	1	1	1	0	0	1
	Status 5	0	0	1	1	1	1	0	1
	Status 6	1	0	1	1	1	0	0	1
Discharging status	Status 7	1	0	0	0	1	1	0	0
	Status 8	1	0	1	1	0	0	0	0
	Status 9	1	0	1	0	1	1	0	0
	Status 10	1	0	1	0	0	0	0	0
	Status 11	1	0	0	0	1	0	0	0
	Status 12	1	0	1	1	1	0	0	0
	Status 13	1	0	1	0	1	0	0	0
	Status 14	1	1	0	0	1	0	0	0
	Status 15	0	0	1	0	1	0	0	0
	Status 16	1	1	0	0	1	1	0	0
	Status 17	1	1	0	0	0	0	0	0
	Status 18	0	0	1	1	0	0	0	0
	Status 19	0	0	1	0	1	1	0	0
	Status 20	0	0	0	0	1	1	0	0

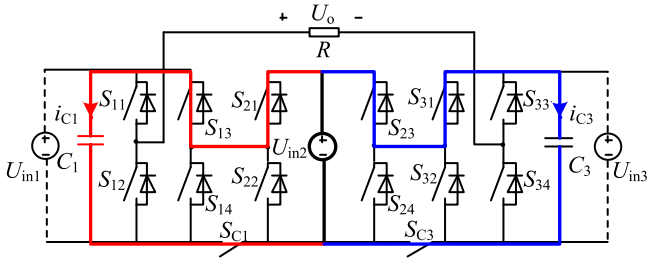

Fig. 3. Equivalent charging circuit for C_1 and C_3.

TABLE II
CHARGING TIME AND OUTPUT VOLTAGE IN DIFFERENT *m*

Modulation value *m*	Charging time	Output voltage
$-1 < m < -2/3$	$(1-\mid m \mid)T_S/2$	$-3U_{in2}$, $-2U_{in2}$,
$-2/3 < m < -1/3$	$T_S/6$	$-2U_{in2}$, $-U_{in2}$
$-1/3 < m < 0$	$T_S/6$	$-U_{in2}$, 0
$0 < m < 1/3$	$T_S/6$	0, $-U_{in2}$
$1/3 < m < 2/3$	$T_S/6$	U_{in2}, $2U_{in2}$
$2/3 < m < 1$	$(1-m)T_S/2$	$2U_{in2}$, $3U_{in2}$

is turned OFF after S_{13}, as illustrated in Fig. 2(c). The charging time is $(1-m)T_S/2$, and the output voltage of the inverter is 2 U_{in2} or 3 U_{in2} and the capacitor voltage U_{C1} would decrease drastically if the modulation wave is increased to 1; however, it would recover in time if the modulation wave is decreased.

Due to the symmetry, the charging time and the output voltage can be easily derived with $m < 0$. Table II gives the charging time and the output voltage in different *m*.

C. Capacitor Discharged Bus Voltage Analysis

To some extent, bus voltages U_{C1} and U_{C3} remain stable. However, they will fluctuate frequently because of the charging or discharging of the capacitor. The influencing factors of U_{C1} and U_{C3} are illustrated as follows. For simplicity, the following assumptions are made: 1) the initial values of U_{C1} and U_{C3} are U_{in2} before discharging; 2) the capacitance of the capacitor C_1 and C_3 is C and the load resistance is R. There are four discharging states for C_1 in a modulation cycle, which are described as follows.

State I: Capacitor C_1 operates individually.

$S_{11}, S_{14}, S_{22}, S_{24}, S_{31}$, and S_{33} are turned ON simultaneously for Status 7 ($S_{11}, S_{14}, S_{21}, S_{23}, S_{32}$, and S_{34} are ON for Status 8). The equivalent circuit of Status 7 is shown in Fig. 4(a). U_{C1} can be expressed as

$$u_{C1}(t) = U_{in2}e^{-\frac{t}{RC}}. \tag{1}$$

State II: Capacitor C_1 and U_{in2} operate simultaneously.

$S_{11}, S_{14}, S_{21}, S_{24}, S_{31}$, and S_{33} are turned ON simultaneously for Status 9 ($S_{11}, S_{14}, S_{21}, S_{24}, S_{32}$, and S_{34} are ON for Status 10). The equivalent circuit of Status 9 is shown in Fig. 4(b). U_{C1} is provided by

$$u_{C1}(t) = U_{in2}(2e^{-\frac{t}{RC}} - 1). \tag{2}$$

State III: Capacitors C_1 and C_3 operate simultaneously.

$S_{11}, S_{14}, S_{22}, S_{24}, S_{31}$, and S_{34} are turned ON simultaneously for Status 11 ($S_{11}, S_{14}, S_{21}, S_{23}, S_{31}$, and S_{34} are ON for Status 12). The equivalent circuit is shown in Fig. 4(c). U_{C1} can be expressed as

$$u_{C1}(t) = U_{in2}e^{-\frac{2t}{RC}}. \tag{3}$$

State IV: Capacitors C_1, C_3, and U_{in2} operate simultaneously.

$S_{11}, S_{14}, S_{21}, S_{24}, S_{31}$, and S_{34} are turned ON simultaneously for Status 13. The equivalent circuit is shown in Fig. 4(d). U_{C1} is provided by

$$u_{C1}(t) = U_{in2}\left(\frac{3}{2}e^{-\frac{2t}{RC}} - \frac{1}{2}\right). \tag{4}$$

The analysis above reveals that the proposed converter has four discharging states. For convenience, the discharging time intervals that belong to the same state are regarded as one continuous discharging time.

1) When $m \in [0, 1/3)$, there are two discharging time intervals in a switching cycle, which are shown in Fig. 2(a). The two time intervals can be deduced easily as $T_1 = T_2 = m/(2f_S)$. According to (1), the voltage variation across C_1 can be expressed as

$$\Delta u_1 = U_{in2} - U_{in2}e^{-\frac{m}{f_S RC}}. \tag{5}$$

2) When $m \in [1/3, 2/3)$, there are six discharging time intervals in a switching cycle, which are shown in Fig. 2(b). Capacitor C_1 and U_{in2} discharge simultaneously during T_1 and T_6. Capacitor C_1 discharges individually during T_2 and T_5. Capacitors C_1 and C_3 discharge simultaneously during T_3 and T_4. The time intervals can be achieved easily as follows: $T_1 = T_3 = T_4 = T_6 = (3m-1)/(6f_S), T_2 = T_5 = (2-3m)/(6f_S)$.

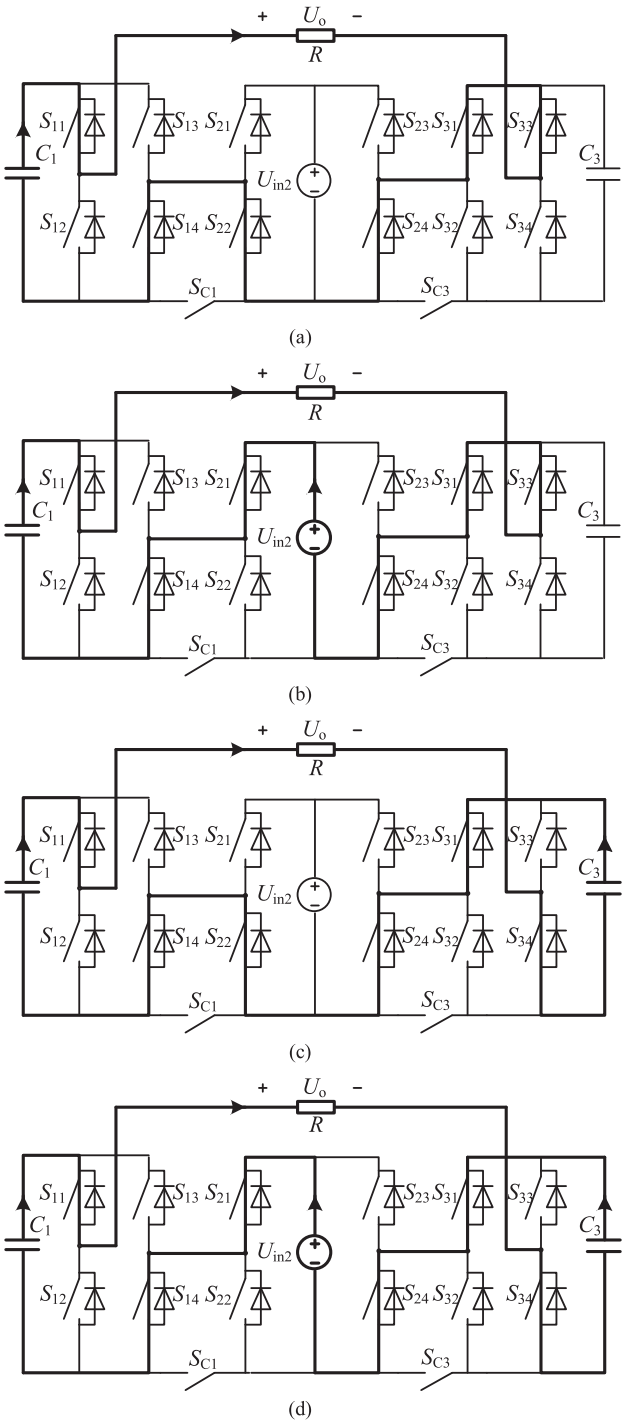

Fig. 4. Capacitor discharging states. (a) C_1 operates individually. (b) C_1 and U_{in2} operate simultaneously. (c) C_1 and C_3 operate simultaneously. (d) C_1, C_3, and U_{in2} operate simultaneously.

In reference to (1) to (3), the voltage variation across C_1 can be expressed as

$$\Delta u_{21} = 2U_{\text{in2}}\left(1 - \text{e}^{-\frac{3m-1}{3f_S RC}}\right) \tag{6}$$

$$\Delta u_{22} = U_{\text{in2}}\left(1 - \text{e}^{-\frac{2-3m}{3f_S RC}}\right) \tag{7}$$

$$\Delta u_{23} = U_{\text{in2}}\left(1 - \text{e}^{-\frac{6m-2}{3f_S RC}}\right). \tag{8}$$

From (6) to (8), we obtain

$$\Delta u_2 = \Delta u_{21} + \Delta u_{22} + \Delta u_{23} = U_{\text{in2}}\left(4 - 2\text{e}^{-\frac{3m-1}{3f_S RC}} - \text{e}^{-\frac{2-3m}{3f_S RC}} - \text{e}^{-\frac{6m-2}{3f_S RC}}\right). \tag{9}$$

3) When $m \in [2/3,\ 1)$, there are ten discharging time intervals in a switching cycle, which are shown in Fig. 2(c). Capacitors C_1, C_3, and U_{in2} discharge simultaneously during T_1, T_3, T_5, T_6, T_8, and T_{10}. Capacitor C_1 and U_{in2} discharge simultaneously during T_2 and T_7. Capacitors C_1 and C_3 discharge simultaneously during T_4 and T_9. The time intervals can be deduced easily as follows: $T_1 = T_3 = T_5 = T_6 = T_8 = T_{10} = (3m-2)/(6f_S), T_2 = T_4 = T_7 = T_9 = (1-m)/(2f_S)$. According to (2)–(4), the voltage variation across C_1 is provided by

$$\Delta u_{31} = \frac{3}{2}U_{\text{in2}}\left(1 - \text{e}^{-\frac{6m-4}{f_S RC}}\right) \tag{10}$$

$$\Delta u_{32} = 2U_{\text{in2}}\left(1 - \text{e}^{-\frac{1-m}{f_S RC}}\right) \tag{11}$$

$$\Delta u_{33} = U_{\text{in2}}\left(1 - \text{e}^{-\frac{2-2m}{f_S RC}}\right). \tag{12}$$

From (10) to (12), we obtain

$$\Delta u_3 = \Delta u_{31} + \Delta u_{32} + \Delta u_{33} = U_{\text{in2}}\left(\frac{9}{2} - \frac{3}{2}\text{e}^{-\frac{6m-4}{f_S RC}} - 2\text{e}^{-\frac{1-m}{f_S RC}} - \text{e}^{-\frac{2-2m}{f_S RC}}\right). \tag{13}$$

In (5), (9), and (13), the capacitor voltage variation Δu is a function of modulation value m, switching frequency f_S, load resistance R, capacitance C_1, and source voltage U_{in2}.Δu decreases when switching frequency f_S, load resistance R, or capacitance C_1 increases. The capacitor voltage variation for different modulation values and frequencies under the condition of $U_{in2} = 136$ V, $R = 50\,\Omega$, and $C = 4700\ \mu$F is drawn in Fig. 5. A large switching frequency should be selected to achieve a small capacitor voltage ripple and improve the steady-state performance of the system.

IV. Current and Voltage on Charging Switch

A. Charging Current and Loss Analysis

Given that U_{C1} and U_{C3} are almost zero in the initial state, the charging current would reach the maximum at system startup. Excessive spike charging current will damage the capacitor and cause the converter to exhibit inefficiency. A current limitation resistor is normally utilized to reduce the charging current but is not discussed in the following analysis.

The charging circuit for C_1 [see Fig. 6(a)] contains only power switches and capacitor, which can be represented by a RC circuit [see Fig. 6(b)]. For simplicity, the following assumptions are made: 1) all power switches are insulated-gate bipolar transistors (IGBTs), 2) V_{CE} is the sum of the forward conduction voltage for S_{21} and S_{C1_1} and V_{FM} is the sum of the diode forward voltage

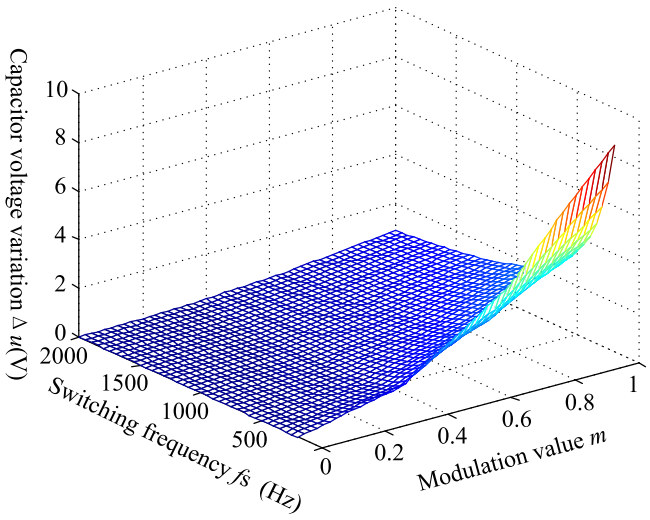

Fig. 5. Scope of capacitor voltage variation at different modulation values and frequencies.

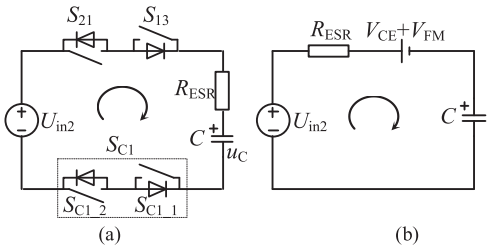

Fig. 6. Circuit and equivalent circuit of the charging process. (a) Charging circuit. (b) Equivalent charging circuit.

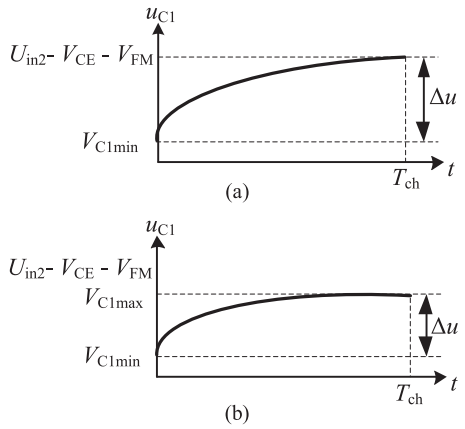

Fig. 7. Capacitor voltage waveforms of charging process. (a) Full charging. (b) Partial charging.

for S_{13} and S_{C1_2}, and 3) R_{ESR} represents the equivalent series resistance (ESR) of the capacitor.

The capacitor voltage waveforms of charging process are illustrated in Fig. 7. V_{C1min} denotes the initial capacitor voltage and V_{C1max} represents the final capacitor voltage. The capacitor charging process can be classified into two conditions, namely, full charging and partial charging. In [24], full charging is defined as one that has a charging time period longer than four times the charging time constant, i.e., $T_{ch} \geq 4\tau_{ch}$, and partial charging corresponds to $T_{ch} < 4\tau_{ch}$, where $\tau_{ch} = R_{ESR}C$. In full charging, the capacitor is charged to the steady-state voltage $U_{in2} - V_{CE} - V_{FM}$, as shown in Fig. 7(a). In partial charging, the capacitor is charged to a voltage less than $U_{in2} - V_{CE} - V_{FM}$, as shown in Fig. 7(b).

The instantaneous capacitor voltage and current can be given by

$$\begin{cases} u_{C1}(t) = V_{C1max} + (V_{C1min} - V_{C1max})e^{-\frac{t}{R_{ESR}C}} \\ i_{C1}(t) = \frac{V_{C1max} - V_{C1min}}{R_{ESR}} e^{-\frac{t}{R_{ESR}C}} = \frac{\Delta u}{R_{ESR}} e^{-\frac{t}{R_{ESR}C}} \end{cases}. \quad (14)$$

The maximum charging current can be expressed by

$$i_{C1\,max} = \frac{\Delta u_{max}}{R_{ESR}}. \quad (15)$$

From Fig. 5, the capacitor voltage variation Δu is a function of modulation value m at a certain switching frequency f_S, load resistance R, capacitance C, and source voltage U_{in2}. Δu increases when m increases.

Therefore, we get the peak current

$$i_{C1\,max} = \frac{U_{in2}\left(\frac{9}{2} - \frac{3}{2}e^{-\frac{6m-4}{f_S RC}} - 2e^{-\frac{1-m}{f_S RC}} - e^{-\frac{2-2m}{f_S RC}}\right)\Big| m = m_{max}}{R_{ESR}}. \quad (16)$$

Charging loss can be expressed as follows:

$$P_{loss} = \frac{1}{T_S}\int_0^{T_{ch}} (i_{C1}^2(t)R_{ESR} + i_{C1}(t)(V_{CE} + V_{FM}))dt \quad (17)$$

where T_{ch} is the charging time, for $m \in (0, 2/3), T_{ch} = T_S/6$, for $m \in (2/3, 1), T_{ch} = (1-m)T_S/2$.

Substituting (14) into (17), we have

$$P_{loss} = \frac{f_S C\Delta u^2}{2R_{ESR}}\left(1 - e^{-\frac{2T_{ch}}{R_{ESR}C}}\right) + f_S C\Delta u(V_{CE} + V_{FM})\left(1 - e^{-\frac{T_{ch}}{R_{ESR}C}}\right). \quad (18)$$

For a given m, the corresponding capacitor voltage can be deduced with (5), (9), and (13). Charging loss can be calculated by (18). The charging loss for different modulation values and frequencies under the condition of $U_{in2} = 136$ V, $R = 50\,\Omega$ and $C = 4700\,\mu$F is drawn in Fig. 8. When the modulation value m becomes larger, the charging loss increases rapidly at a small f_S. But in general, with the increase of switching frequency, the switching loss will be greatly increased. Thus, the switching frequency f_S can be chosen as more than 1.5 kHz to ensure a small capacitor voltage variation and charging loss across the entire modulation index, as shown in Figs. 5 and 8. In this study, the switching frequency f_S is selected as 1.667 kHz eventually so that the output voltage has a switching pattern with 10 kHz.

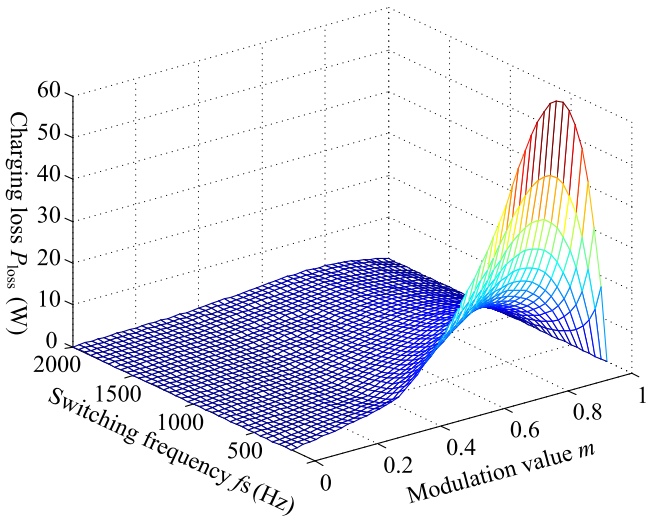

Fig. 8. Extent of charging loss at different modulation amplitudes and frequencies.

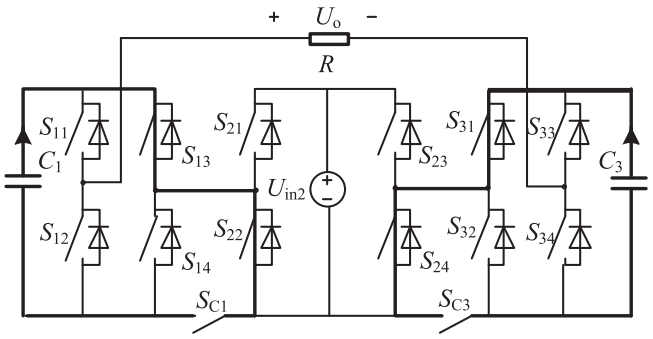

Fig. 9. Voltage of S_{C1} in state II.

B. Charging Switch Voltage Analysis

By introducing the charging-switch pairs, the proposed cascaded seven-level inverter can operate well with only a single dc input source. It is necessary to analyze the charging-switch pair's voltage stress and S_{C1} was taken as an example for the voltage analysis. There are four voltage states for S_{C1} in a modulation cycle, which are described as follows.

State I: S_{13}, S_{21}, and S_{C1} are turned ON. The positive sides of C_1 and U_{in2} are connected directly. Input source U_{in2} can charge C_1 by introducing S_{C1}, as shown in Fig. 3. The voltage of S_{C1} is zero.

State II: S_{13} and S_{22} are turned ON, and S_{C1} is turned OFF. The voltage of S_{C1} is $-S_{C1}$, as shown in Fig. 9.

State III: In Fig. 4(b) and (d), S_{14} and S_{21} are turned ON, and the voltage of S_{C1} is U_{in2}.

State IV: In Fig. 4(a) and (c), S_{14} and S_{22} are turned ON and the voltage of S_{C1} is zero.

States I–IV indicate that the voltage of S_{C1} is 0, the capacitor voltage U_{C1} or the source voltage U_{in2}. Therefore, the proposed converter has low voltage stress on each switch, which resulted in low cost.

TABLE III
SYSTEM SIMULATION PARAMETERS

Circuit parameters	Value
U_{in2}	136 V
fs	1.667 kHz
R	50 Ω
L	60 mH
C_1/C_3	4700 μF

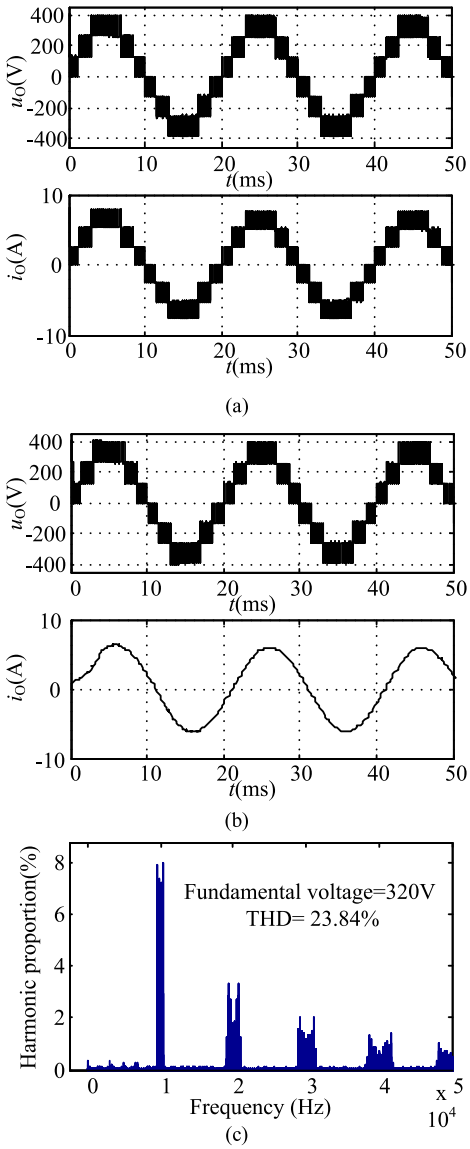

Fig. 10. Output voltage and current waveforms. (a) At resistive load. (b) At inductive load. (c) THD value of the output voltage.

V. Simulation and Experimental Verifications

A. Simulation Results

The simulation parameters of the proposed converter are given in Table III.

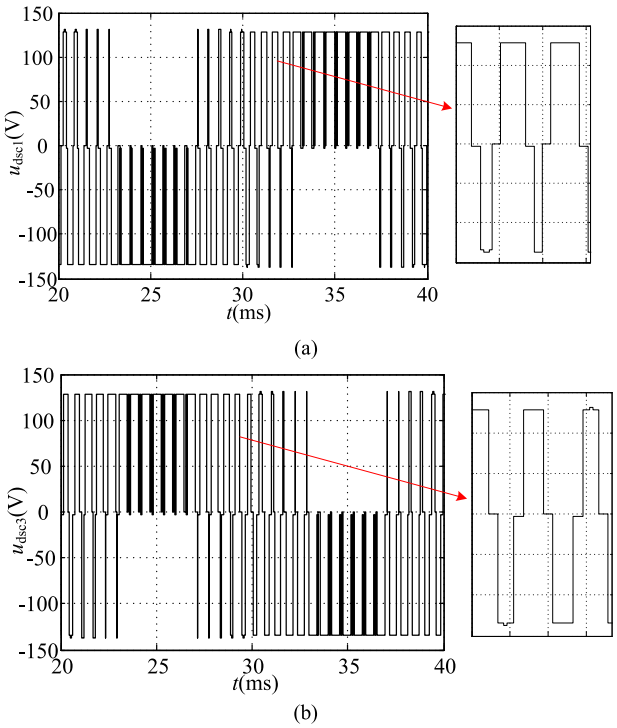

Fig. 11. Voltage waveforms of the charging-switch. (a) S_{C1}. (b) S_{C3}.

The output voltage and current waveforms for resistive and inductive load are given in Fig. 10. The output current lags behind the voltage at inductive load. And the current is smooth due to the filter inductance. As shown in Fig. 10(c), the harmonic is mainly concentrated on the octave band and sidebands at 10 kHz. The THD value of u_O is 23.84%.

The ideal voltage waveforms of the charging-switch pairs S_{C1} and S_{C3} are shown in Fig. 11. It can be seen that the voltage states for S_{C1} and S_{C3} are 0, U_{in2} or $-U_{in2}$ in a modulation cycle. The voltage stress of the charging-switch pair is within the source voltage, which verifies the theoretical analysis.

The capacitor voltage and the charging current waveforms of capacitors C_1 with the ESR value of 5 mΩ in the full charging process are shown in Fig. 12(a). In the simulation model, V_{CE} and V_{FM} are selected as 3 V. It can be seen that the capacitor voltage u_{C1} reaches the steady-state voltage $U_{in2} - V_{CE} - V_{FM}$, which is about 130 V and the charging current has become zero at the end of the charging time. Besides, the capacitor voltage variation Δu increases when the modulation value m increases in a modulation cycle. According to the formula (13) and (16), the theoretical value Δu_{max} is calculated as 0.75 V and Δi_{C1max} is 150 A at the maximum value of $m = 0.833$. From Fig. 12(a), the simulation value Δu_{max} is about 0.7 V and Δi_{C1max} equals 140 A, which are in agreement with the theoretical analysis. The peak charging current can be reduced by increasing the ESR. The waveforms with the ESR value of 200 mΩ in the partial process are illustrated in Fig. 12(b). Due to a large R_{ESR}, the peak charging current can be limited. However, u_{C1} cannot reach the steady-state value. In this situation, the charge–discharge process is so complicated that we cannot get the specific expression of the peak current.

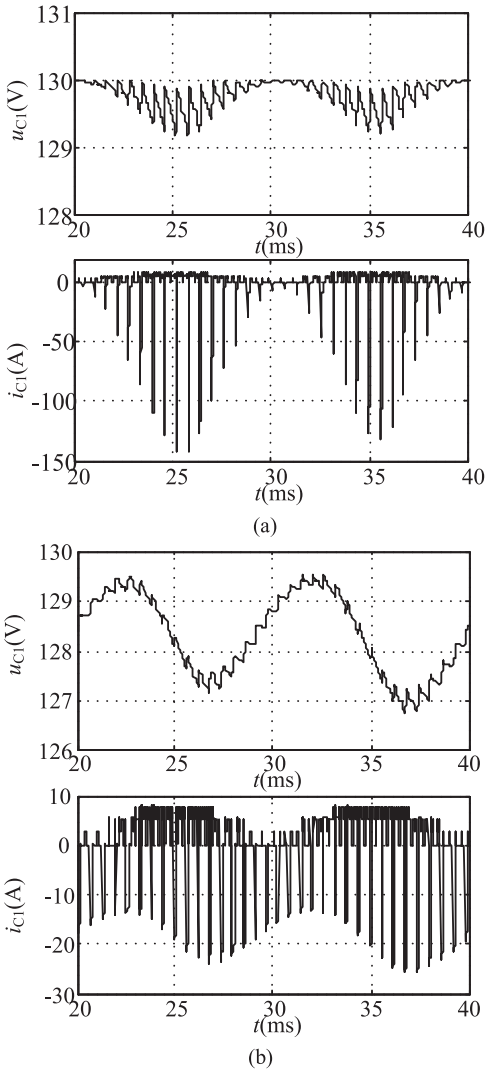

Fig. 12. Capacitor voltage and the charging current waveforms of capacitors C_1. (a) $R_{ESR} = 5$ mΩ. (b) $R_{ESR} = 200$ mΩ.

B. Experimental Results

As shown in Fig. 13, a 1-kW experimental prototype was built to verify the feasibility and effectiveness of the proposed topology with a single dc source. The specifications of the prototype are provided in Table IV. The control block diagram is given in Fig. 14.

The main experimental waveforms are illustrated in Fig. 15. The output voltage and current waveforms at 1 kW of resistive load are given in Fig. 15(a). As shown in Fig. 15(b), the waveforms of u_{C1} and u_{C3} are less than U_{in2} and the difference between them is almost 5–7 V, which is almost the sum of four IGBT conduction voltage drop. As seen in the enlarged waveform of u_{C1}, the capacitor charging process belongs to the partial charging. The driving voltage and drain-to-source voltage of S_{C1}

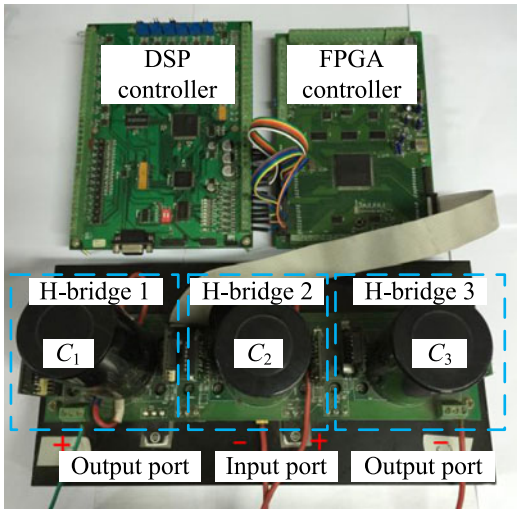

Fig. 13. Prototype for the experiment.

TABLE IV
UTILIZED COMPONENTS AND PARAMETERS

Components and parameters	Value
Main control chip	TMS320LF2407A + XC3S400
Charging-switch pairs (IGBT)	FGH40N60 (40 A, 600 V)
Main switches (IGBT)	FGH20N60 (20 A, 600 V)
Capacitances C_1 and C_3 (μF)	4700
Load voltage $uo_{\rm rms}$ (V)	220 (PF = 1)
Load side inductance L (mH)	60
Output frequency fo (Hz)	50
Switching frequency $f_{\rm S}$ (kHz)	1.667
Equivalent output switching frequency $f_{\rm ES}$ (kHz)	10
Modulation ratio	0.833

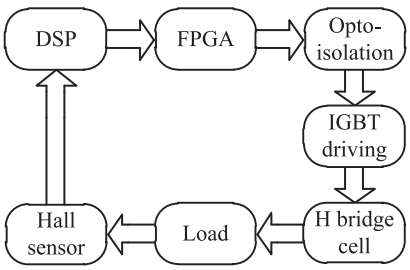

Fig. 14. Control block diagram of the single-supply cascaded seven-level inverter.

are shown in Fig. 15(c). The voltage across a charging-switch pair is within the source voltage. The output voltage and current waveform at inductive load are given in Fig. 15(d) and (e). The experimental results verify the feasibility and effectiveness of the proposed single-supply cascaded seven-level inverter.

The curves of efficiency versus power in the proposed and traditional cascaded seven-level inverters with the same circuit parameters are illustrated in Fig. 16. The values of the two curves are basically in agreement and both are more than 90%. However, the efficiency value of the proposed inverter is lower than that of the traditional inverter because of the charging loss.

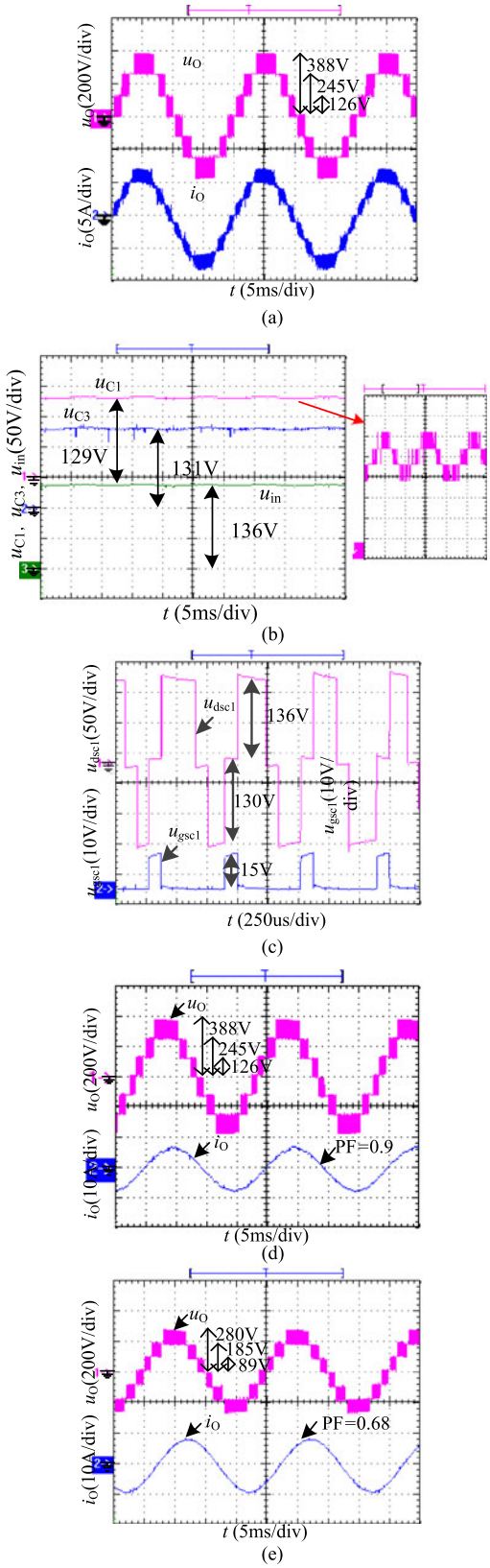

Fig. 15. Experimental waveforms of the proposed inverter. (a) Output voltage and current at resistive load. (b) $U_{\rm C1}, U_{\rm C3}$ and $U_{\rm in2}$. (c) Driving voltage and drain-to-source voltage of $S_{\rm C1}$. (d) Output voltage and current at inductive load (PF = 0.9). (e) Output voltage and current at inductive load (PF = 0.68).

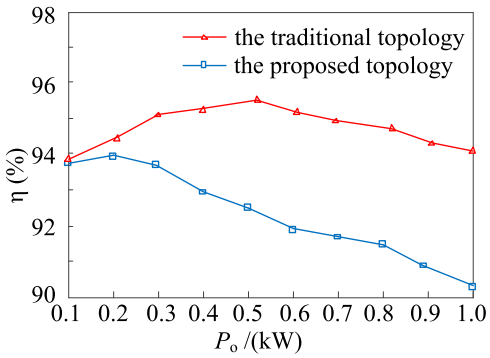

Fig. 16. Efficiency versus power in the proposed and traditional topologies.

VI. Conclusion

A novel single dc source cascaded seven-level inverter integrating switched-capacitor technique was developed in this paper. In the proposed topology, the transformerless charging circuit only contains power switches and capacitors, and the charging time is independent of the load. The operation principle and the charging–discharging characteristic analysis were investigated in depth. With the common CPS-SPWM strategy, the sinusoidal output voltage can be well obtained. Moreover, the capacitors are properly charged without complex voltage balancing control algorithm. The peak charging current and the charging loss can be reduced with appropriate circuit parameters. The proposed topology has the features of modularity, low cost, and simplicity of control and makes it attractive in dc–ac power applications. A 1-kW experimental prototype verifies the feasibility of the proposed inverter. The proposed inverter is also suitable for photovoltaic-battery multi-input application with high redundancy.

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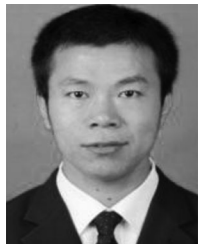

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